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LERNER GREENBERG STEMER LLP			ALHJIA, SAIF A	
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			2128	

DATE MAILED: 10/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/622,933

Applicant(s)

LIAU, CHEE HONG

Examiner

Saif A. Alhija

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 18 July 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-36 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-36 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 18 July 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
- 1) ☒ Certified copies of the priority documents have been received.
 - 2) ☐ Certified copies of the priority documents have been received in Application No. _____.
 - 3) ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date 9/2/05, 7/18/03.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-36 have been presented for examination.

PRIORITY

2. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d).

Information Disclosure Statement

3. The information disclosure statements (IDS) submitted on 2 September 2005 and 18 July 2003 are in compliance with the provisions of 37 CFR 1.97. Accordingly, the Examiner has considered the IDS' as to the merits.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

MPEP 2106 recites:

The claimed invention as a whole must accomplish a practical application. That is, it must produce a "useful, concrete and tangible result" State Street 149 F.3d at 1373, 47 USPQ2d at 1601-02. A process that consists solely of the manipulation of an abstract idea is not concrete or tangibles. See In re Warmerdam, 33 F.3d 1354, 1360, 31 USPQ2d 1754, 1759 (Fed.Cir. 1994). See also Schrader, 22 F.3d at 295, 30 USPQ2d at 1459.

4. **Claims 1-36 are rejected** under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

- i) The claims recite the steps of selecting, applying, approximating, adapting, and comparing. These steps appear to be a manipulation of data and/or software modules. It is unclear if the

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resultant of the claims is stored, provided to a user, etc. As such the claims do not produce a useful, concrete, and tangible result.

ii) The claims also appear to recite a computer program. It should be noted that code (i.e., a computer software program) does not do anything per se. Instead, it is the code stored on a computer that, *when executed*, instructs the computer to perform various functions. The following claim is a generic example of a proper computer program product claim;

A computer program product embodied on a computer-readable medium and comprising code that, when executed, causes a computer to perform the following:

Function A
Function B
Function C, etc...

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. **Claims 1-36 are rejected** under 35 U.S.C. 102(b) as being clearly anticipated by Yao “Evolving Artificial Neural Networks”, hereafter referred to as Yao.

Regarding Claim 1:

Yao discloses A method of approximating a behavior of an integrated circuit, the method which comprises the steps of:

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(a) applying a set of test patterns to a system for one of testing and simulating an integrated circuit; (Abstract. Page 1423-1424, Section I, A-C. Page 1425, Section II. Page 1434, Section III, D. Page 1438, Section V, C-D. Page 1439, Conclusion)

(b) applying the set of test patterns to a neural network; (Abstract. Page 1423-1424, Section I, A-C. Page 1425, Section II. Page 1434, Section III, D. Page 1438, Section V, C-D. Page 1439, Conclusion)

(c) comparing outputs of the system for one testing and simulating the integrated circuit and outputs of the neural network for providing a comparison result; and (Abstract. Page 1423-1424, Section I, A-C. Page 1425, Section II. Page 1434, Section III, D. Page 1438, Section V, C-D. Page 1439, Conclusion)

(d) adapting parameters of the neural network to approximate a behavior of the integrated circuit based the comparison result. (Abstract. Page 1423-1424, Section I, A-C. Page 1425, Section II. Page 1434, Section III, D. Page 1438, Section V, C-D. Page 1439, Conclusion)

Regarding Claim 2:

Yao discloses The method according to claim 1, which comprises: using, as the system for one of testing and simulating the integrated circuit, an automatic test equipment (ATE); and applying the set of test patterns to the integrated circuit via the automatic test equipment. (Abstract. Page 1423-1424, Section I, A-C. Page 1425, Section II. Page 1434, Section III, D. Page 1438, Section V, C-D. Page 1439, Conclusion)

Regarding Claim 3:

Yao discloses The method according to claim 2, which comprises implementing the neural network in the automatic test equipment. (Abstract. Page 1423-1424, Section I, A-C. Page 1425,

Section II. Page 1434, Section III, D. Page 1438, Section V, C-D. Page 1439, Conclusion)

Regarding Claim 4:

Yao discloses The method according to claim 1, which comprises generating the set of test patterns on a random basis. (Abstract. Page 1423-1424, Section I, A-C. Page 1425, Section II. Page 1434, Section III, D. Page 1438, Section V, C-D. Page 1439, Conclusion)

Regarding Claim 5:

Yao discloses The method according to claim 1, wherein step (d) includes adapting inter-unit weights of the neural network through back-propagation. (Abstract. Page 1423-1424, Section I, A-C. Page 1425, Section II. Page 1434, Section III, D. Page 1438, Section V, C-D. Page 1439, Conclusion)

Regarding Claim 6:

Yao discloses The method according to claim 1, which comprises repeating steps (a) to (d) until a level of adaptation in step (d) falls below a given value. (Abstract. Page 1423-1424, Section I, A-C. Page 1425, Section II. Page 1434, Section III, D. Page 1438, Section V, C-D. Page 1439, Conclusion)

Regarding Claim 7:

Yao discloses The method according to claim 5, which comprises storing data representing predetermined neural network parameters after terminating a repetition of steps (a) to (d). (Abstract. Page 1423-1424, Section I, A-C. Page 1425, Section II. Page 1434, Section III, D. Page 1438, Section V, C-D. Page 1439, Conclusion)

Regarding Claim 8:

Yao discloses A method of selecting test patterns, the method which comprises the steps of: (a) approximating a behavior of an integrated circuit by applying a set of test patterns to a system for one of testing and simulating the integrated circuit, applying the set of test patterns to a neural network, comparing outputs of the system for one testing and simulating the integrated circuit and outputs of the neural network for providing a comparison result, and adapting parameters of the neural network in order to approximate the behavior of the integrated circuit based the comparison result; (b) applying a test pattern to the neural network whose parameters have been adapted to approximate the behavior of the integrated circuit in accordance with step (a); (c) processing an output of the neural network to determine whether given criteria are met; and (d) selecting the test pattern for storage if the given criteria are met. (Abstract. Page 1423-1424, Section I, A-C. Page 1425, Section II. Page 1434, Section III, D. Page 1438, Section V, C-D. Page 1439, Conclusion)

Regarding Claim 9:

Yao discloses The method according to claim 8, which comprises repeating steps (b) to (d) until a given number of test patterns have been stored. (Abstract. Page 1423-1424, Section I, A-C. Page 1425, Section II. Page 1434, Section III, D. Page 1438, Section V, C-D. Page 1439, Conclusion)

Regarding Claim 10:

Yao discloses The method according to claim 8, which comprises concluding that the given criteria are met if a value of a given parameter of a signal output by the neural network in response to applying the test pattern exceeds a reference value. (Abstract. Page 1423-1424, Section I, A-C. Page 1425, Section II. Page 1434, Section III, D. Page 1438, Section V, C-D. Page 1439, Conclusion)

Regarding Claim 11:

Yao discloses The method according to claim 10, which comprises: (e) applying a further set of test patterns to the integrated circuit by using an automatic test equipment; (f) measuring values of the given parameter of output signals generated by the integrated circuit in response to step (e); and (g) concluding that the given criteria are met if the value of the given parameter of the signal output by the neural network in response to applying a test pattern exceeds the reference value and all values measured in step (f). (Abstract. Page 1423-1424, Section I, A-C. Page 1425, Section II. Page 1434, Section III, D. Page 1438, Section V, C-D. Page 1439, Conclusion)

Regarding Claim 12:

Yao discloses The method according to claim 11, which comprises generating the further set of test patterns on a random basis. (Abstract. Page 1423-1424, Section I, A-C. Page 1425, Section II. Page 1434, Section III, D. Page 1438, Section V, C-D. Page 1439, Conclusion)

Regarding Claim 13:

Yao discloses The method according to claim 10, which comprises using a dynamic current as the given parameter. (Abstract. Page 1423-1424, Section I, A-C. Page 1425, Section II. Page 1434, Section III, D. Page 1438, Section V, C-D. Page 1439, Conclusion)

Regarding Claim 14:

Yao discloses The method according to claim 8, which further comprises: (h) generating a test pattern population formed of a plurality of test patterns; (i) applying each test pattern of the test pattern population to the neural network; (j) processing, for each test pattern, the output of the neural network to determine a value of a given parameter; and (k) allocating each test pattern to one of a plurality of classification groups in accordance with the value of the given parameter determined in step (j).

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(Abstract. Page 1423-1424, Section I, A-C. Page 1425, Section II. Page 1434, Section III, D. Page 1438, Section V, C-D. Page 1439, Conclusion)

Regarding Claim 15:

Yao discloses The method according to claim 14, which comprises repeating steps (h) to (k) using a new test pattern population formed of test patterns included in a selected one of the classification groups. **(Abstract. Page 1423-1424, Section I, A-C. Page 1425, Section II. Page 1434, Section III, D. Page 1438, Section V, C-D. Page 1439, Conclusion)**

Regarding Claim 16:

Yao discloses The method according to claim 15, which comprises using, as the selected one of the classification groups, test patterns that approximate a set of worst case input parameters of operation of the integrated circuit. **(Abstract. Page 1423-1424, Section I, A-C. Page 1425, Section II. Page 1434, Section III, D. Page 1438, Section V, C-D. Page 1439, Conclusion)**

Regarding Claim 17:

Yao discloses The method according to claim 8, which comprises: repeating steps (b) to (d) a number of times; applying the test patterns selected in each step (d) to a simulator for simulating the integrated circuit; processing an output of the simulator to determine whether further given criteria are met; and selecting for storage those test patterns that meet the further given criteria. **(Abstract. Page 1423-1424, Section I, A-C. Page 1425, Section II. Page 1434, Section III, D. Page 1438, Section V, C-D. Page 1439, Conclusion)**

Regarding Claim 18:

Yao discloses The method according to claim 8, which comprises: repeating steps (b) to (d) a number of times; applying test patterns selected in each repetition of step (d) to the integrated circuit by using an automatic test equipment; processing an output of the automatic test equipment to determine whether further given criteria are met; and selecting for storage those test patterns which meet the further given criteria. (Abstract. Page 1423-1424, Section I, A-C. Page 1425, Section II. Page 1434, Section III, D. Page 1438, Section V, C-D. Page 1439, Conclusion)

Regarding Claim 19:

Yao discloses The method according to claim 8, which comprises using, as the given criteria, a representation of an approximation of a worst case mode of operation of the integrated circuit. (Abstract. Page 1423-1424, Section I, A-C. Page 1425, Section II. Page 1434, Section III, D. Page 1438, Section V, C-D. Page 1439, Conclusion)

Regarding Claim 20:

Yao discloses A method of simulating an integrated circuit, the method which comprises the steps of: selecting test patterns by, in a first step, applying a test pattern to a neural network whose parameters have been adapted to approximate a behavior of an integrated circuit by applying a set of test patterns to a system for one of testing and simulating the integrated circuit, applying the set of test patterns to a neural network, and comparing outputs of the system for one of testing and simulating the integrated circuit and outputs of the neural network, and, in a second step, processing an output of the neural network to determine whether given criteria are met and selecting a test pattern if the given criteria are met; and applying test patterns that have been selected to a simulator for simulating the integrated circuit. (Abstract. Page 1423-1424, Section I, A-C. Page 1425, Section II. Page 1434, Section III, D. Page 1438, Section V, C-D. Page 1439, Conclusion)

Regarding Claim 21:

Yao discloses A method of testing an integrated circuit, the method which comprises the steps of: selecting test patterns by, in a first step, applying a test pattern to a neural network whose parameters have been adapted to approximate a behavior of an integrated circuit by applying a set of test patterns to a system for one of testing and simulating the integrated circuit, applying the set of test patterns to a neural network, and comparing outputs of the system for one of testing and simulating the integrated circuit and outputs of the neural network, and, in a second step, processing an output of the neural network to determine whether given criteria are met and selecting a test pattern if the given criteria are met; and applying test patterns that have been selected to the integrated circuit by using an automatic test equipment. (Abstract. Page 1423-1424, Section I, A-C. Page 1425, Section II. Page 1434, Section III, D. Page 1438, Section V, C-D. Page 1439, Conclusion)

Regarding Claim 22:

Yao discloses A method of providing a test pattern for one of a simulation and a test of a layout of an integrated circuit, the method which comprises the steps of: (A) providing a set of test patterns that have been selected by, in a first step, applying a test pattern to a neural network whose parameters have been adapted to approximate a behavior of an integrated circuit by applying a set of test patterns to a system for one of testing and simulating an integrated circuit, applying the set of test patterns to a neural network, and comparing outputs of the system for one of testing and simulating the integrated circuit and outputs of the neural network, and, in a second step, processing an output of the neural network to determine whether given criteria are met and selecting a test pattern if the given criteria are met; and (B) applying the set of test patterns to the integrated circuit by using an automatic test equipment (ATE); (C) determining outputs of the integrated circuit; (D) processing the outputs to determine whether given test

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criteria are met; and (E) depending on a determination in step (D), generating a new set of test patterns based on the set of test patterns provided by step (A) by using a genetic algorithm. (**Abstract. Page 1423-1424, Section I, A-C. Page 1425, Section II. Page 1434, Section III, D. Page 1438, Section V, C-D. Page 1439, Conclusion**)

Regarding Claim 23:

Yao discloses The method according to claim 22, which comprising repeating steps (B) to (E) until the given test criteria are met. (**Abstract. Page 1423-1424, Section I, A-C. Page 1425, Section II. Page 1434, Section III, D. Page 1438, Section V, C-D. Page 1439, Conclusion**)

Regarding Claim 24:

Yao discloses The method according to claim 22, which comprises repeating steps (B) to (E) until a condition is met, the condition being selected from the group consisting of meeting the given test criteria and repeating steps (B) to (E) a given number of times. (**Abstract. Page 1423-1424, Section I, A-C. Page 1425, Section II. Page 1434, Section III, D. Page 1438, Section V, C-D. Page 1439, Conclusion**)

Regarding Claim 25:

Yao discloses The method according to claim 22, which comprises concluding that the given test criteria are met if the set of test patterns is associated with an average fitness above a given value. (**Abstract. Page 1423-1424, Section I, A-C. Page 1425, Section II. Page 1434, Section III, D. Page 1438, Section V, C-D. Page 1439, Conclusion**)

Regarding Claim 26:

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Yao discloses The method according to claim 22, wherein step (E) includes combining at least some of the test patterns according to the genetic algorithm in order to provide the new set of test patterns. **(Abstract. Page 1423-1424, Section I, A-C. Page 1425, Section II. Page 1434, Section III, D. Page 1438, Section V, C-D. Page 1439, Conclusion)**

Regarding Claim 27:

Yao discloses The method according to claim 26, which further comprises: selecting test patterns from the set of test patterns according to given selection criteria in order to provide selected test patterns; and combining the selected test patterns according to the genetic algorithm to provide the new set of test patterns. **(Abstract. Page 1423-1424, Section I, A-C. Page 1425, Section II. Page 1434, Section III, D. Page 1438, Section V, C-D. Page 1439, Conclusion)**

Regarding Claim 28:

Yao discloses The method according to claim 27, which comprises selecting a test pattern if the test pattern is associated with a fitness value greater than a reference value. **(Abstract. Page 1423-1424, Section I, A-C. Page 1425, Section II. Page 1434, Section III, D. Page 1438, Section V, C-D. Page 1439, Conclusion)**

Regarding Claim 29:

Yao discloses The method according to claim 27, which comprises selecting a test pattern if the test pattern is associated with a highest fitness value of all unselected test patterns. **(Abstract. Page 1423-1424, Section I, A-C. Page 1425, Section II. Page 1434, Section III, D. Page 1438, Section V, C-D. Page 1439, Conclusion)**

Regarding Claim 30:

Yao discloses The method according to claim 27, which comprises selecting a test pattern if the test pattern is associated with a highest fitness value of all unselected test patterns, and repeating the selecting step until a given percentage of test patterns has been selected. **(Abstract. Page 1423-1424, Section I, A-C. Page 1425, Section II. Page 1434, Section III, D. Page 1438, Section V, C-D. Page 1439, Conclusion)**

Regarding Claim 31:

Yao discloses The method according to claim 29, wherein step (E) includes: (F) sorting selected test patterns according to an order of associated fitness values; (G) randomly selecting parent test patterns from test patterns as sorted in step (F); and (H) combining selected ones of the parent test patterns. **(Abstract. Page 1423-1424, Section I, A-C. Page 1425, Section II. Page 1434, Section III, D. Page 1438, Section V, C-D. Page 1439, Conclusion)**

Regarding Claim 32:

Yao discloses The method according to claim 22, which comprises using at least one element selected from the group consisting a mutation, a crossing over, and a re-combination for the genetic algorithm. **(Abstract. Page 1423-1424, Section I, A-C. Page 1425, Section II. Page 1434, Section III, D. Page 1438, Section V, C-D. Page 1439, Conclusion)**

Regarding Claim 33:

Yao discloses The method according to claim 22, wherein the step (A) includes providing a plurality of sets of test patterns such that each of the sets of test patterns is included in a test pattern

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population. (Abstract. Page 1423-1424, Section I, A-C. Page 1425, Section II. Page 1434, Section III, D. Page 1438, Section V, C-D. Page 1439, Conclusion)

Regarding Claim 34:

Yao discloses The method according to claim 22, which comprises providing a plurality of test pattern populations and performing steps (B) to (E) for each of the test pattern populations. (Abstract. Page 1423-1424, Section I, A-C. Page 1425, Section II. Page 1434, Section III, D. Page 1438, Section V, C-D. Page 1439, Conclusion)

Regarding Claim 35:

Yao discloses A data processing configuration, comprising: a system for one of testing and simulating an integrated circuit, said system being configured to be supplied with a set of test patterns; a neural network operatively connected to said system for one of testing and simulating the integrated circuit, said neural network being configured to be provided with the set of test patterns; a comparison unit operatively connected to said neural network and said system for one of testing and simulating the integrated circuit, said comparison unit being configured to compare outputs from said system for one of testing and simulating the integrated circuit and from said neural network in order to provide a comparison result; and an adapting unit operatively connected to said comparison unit, said adapting unit being configured to adapt parameters of said neural network in order to approximate a behavior of the integrated circuit based the comparison result. (Abstract. Page 1423-1424, Section I, A-C. Page 1425, Section II. Page 1434, Section III, D. Page 1438, Section V, C-D. Page 1439, Conclusion)

Regarding Claim 36:

Yao discloses A computer-readable medium having computer-executable instructions for performing a method which comprises the steps of: applying a set of test patterns to a system for one of testing and simulating an integrated circuit; applying the set of test patterns to a neural network; comparing outputs of the system for one of testing and simulating the integrated circuit and outputs of the neural network for providing a comparison result; and adapting parameters of the neural network to approximate a behavior of the integrated circuit based the comparison result. (Abstract. Page 1423-1424, Section I, A-C. Page 1425, Section II. Page 1434, Section III, D. Page 1438, Section V, C-D. Page 1439, Conclusion)

Conclusion

7. All Claims are rejected.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Saif A. Alhija whose telephone number is (571) 272-8635. The examiner can normally be reached on M-F, 11:00-7:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini Shah can be reached on (571) 272-2279. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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SAA

September 25, 2006

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